REMARKS

Claims 1-7, 9 and 10 have been amended to improve form. Claims 1-7, 9-13 and 15-19 remain pending in this application.

Claims 1, 9-11, 13 and 16-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell et al. (U.S. Patent No. 6,208,650; hereinafter Hassell) in view of Springer et al. (U.S. Patent No. 4,247,920; hereinafter Springer). The rejection is respectfully traversed.

Claim 1 recites a network device that includes a plurality of receive devices and an external memory interface. Claim 1 recites that the external memory interface is configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory. Claim 1 also recites that the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, where the external memory interface is further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus.

The Office Action admits that Hassell does not disclose an external memory interface that transfers a portion of data received from a first receive device to a first memory and a portion of data received from a second receive to a second memory (Office Action – page 2).

The Office Action, however, states that Springer discloses an external memory interface and an external memory that includes an even memory and an odd memory and

points to col. 1, lines 63-67 for support (Office Action – page 3). The Office Action also states that Springer discloses that the external memory interface includes a first external memory bus and a second external memory bus and that the external memory interface is configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus and points to col. 5, line 34 to col. 6, line 6 for support (Office Action – page 3). The applicants respectfully disagree.

Springer is directed to a system for permitting individual bytes of a two-byte information signal to be stored or retrieved from a single memory space (Springer – col. 1, lines 40-58). Springer at col. 1, lines 63-67 discloses that a memory device in accordance with Springer's invention may be divided into two modules, one designated odd and the other designated even to indicate a logical grouping of addresses.

Springer at col. 5, line 6 to col. 6, line 4 discloses performing a 16-bit memory access to memory modules 22 and 24 (Fig. 1). Springer discloses that a 16-bit memory access to system address will result in an access to both modules 22 and 24 at a module address of N/2 if N is even and access to module 22 at an address defined by an integer part of N/2 and an access to module 24 at an address defined by the integer part of (N+1)/2 if N is odd (col. 5, lines 27-33 and Fig. 1). Therefore, Springer clearly discloses that access to modules 22 and 24 is based on receipt of an existing address signal N on address signal line 34 (See col. 2, lines 60-68). Springer does not disclose generating odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus, as recited in claim 1.

Springer at col. 5, line 34 to col. 6, line 6 provides examples for a 16-bit memory access in which the even address of 230/16 and the odd address of 231/16 are considered. For the even address of 230/16, Springer discloses that the upper 15 bits of the address signal are sent unchanged to the odd memory module 22. Springer also discloses that control circuit 38 receives the least significant address bits via line 70 and the address signal is also fed through incrementor 36. The upper 15 bits of the incremented address signal are then sent to even memory module 24. Springer also states that the upper 15 bits of an even address signal do not change when the 16-bit address signal is incremented by one and as a result, the access to both memory modules 22 and 24 is at location 118 (col. 5, lines 37-53 and Figs. 1 and 2).

For the odd address 231/16, Springer discloses that the upper 15 bits of the address signal are sent unchanged to odd memory module 22, which correspond to a module address of 118. In this case, however, the upper 15 bits of the incremented address signal are changed. As a result, the access to even memory module 24 is at location 119 (col. 5, lines 55 to col. 6, line 2).

These portions of Springer do not disclose generating odd address information when transferring data to a first memory via a first external memory bus and generating even address information when transferring data to a second memory via a second external memory bus, as required by claim 1. In contrast, Springer merely discloses using existing address information received on address signal line 34 to determine a module address associated with accessing memory modules 22 and 24. If the Examiner persists in this argument, the applicants respectfully request that the Examiner explain how using existing

address information received on address signal line 34 to determine a module address is equivalent to the features recited in claim 1.

For at least the reasons discussed above, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 1. Accordingly, withdrawal of the rejection and allowance of claim 1 are respectfully requested.

Claims 9 is dependent on claim 1 and is believed to be allowable for at least the reasons claim 1 is allowable. Accordingly, withdrawal of the rejection and allowance of claim 9 are respectively requested.

Claim 10 recites a method for storing data frame information that includes simultaneously transferring data frame information to at least a first memory and a second memory, wherein the simultaneously transferring includes alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories. The Office Action states that Springer discloses these features and points to col. 2, lines 1-11 for support (Office Action – page 4). The applicants respectfully disagree.

Springer at col. 2, lines 1-11 discloses:

> For an even memory address N, an access is made to a location in each memory module having an address of N/2. For an odd memory address N, the access in the odd module is to a location having an address defined by the integer part of N/2, but the access in the odd module is to a location having an address defined by the integer part of N/2+1. In the first case, the even memory module supplies or receives the upper byte of the information signal, and in the second case, the odd module supplies or receives the upper byte.

This portion of Springer, as best understood by the applicants, merely discloses how to process an incoming address signal N with respect to an odd and even memory module.

This portion of Springer clearly does not disclose alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories, as recited in claim 10. If the Examiner persists in this argument, the applicants respectfully request that the Examiner explain how this portion of Springer can be construed to disclose alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories, as recited in claim 10.

For at least these reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 10. Accordingly, withdrawal of the rejection and allowance of claim 10 are respectfully requested.

Claims 11, 13 and 15 are dependent on claim 10 and are believed to be allowable for at least the reasons claim 10 is allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 11 recites simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices. The Office Action states that Springer discloses this feature and points to col. 2, lines 18-27 for support (Office Action – page 4). The applicants respectfully disagree.

Springer at col. 2, lines 18-27 discloses that an objective of Springer's invention is to provide means for transferring a two-byte information signal into and out of a byte-oriented memory system such that the first and second bytes are associated with sequential storage

locations. This portion of Springer clearly does not disclose simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices, as recited in claim 11.

For at least this additional reason, withdrawal of the rejection and allowance of claim 11 are respectfully requested.

Claim 16 recites a data communication system that includes a plurality of receive devices, a scheduler, a switching device, a first memory and a second memory. Claim 16 recites that the switching device is configured to generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory. The Office Action states that Springer discloses this feature and points to col. 5, line 34 to col. 6, line 6 for support (Office Action – page 5). The applicants respectfully disagree.

Similar to the discussion above with respect to claim 1, this portion of Springer does not disclose generating odd addresses for data transferred to a first memory and even addresses for data transferred to a second memory, as recited in claim 16. Rather, Springer merely discloses using existing address information received on address signal line 34 to determine a module address associated with accessing memory modules 22 and 24.

For at least these reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 16. Accordingly, withdrawal of the rejection and allowance of claim 16 are respectfully requested.

Claims 17-19 are dependent on claim 16 and are believed to be allowable for at least the reasons claim 16 is allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 18 recites that the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses. The Office Action states that Springer discloses this feature and points to col. 2, lines 1-11 for support (Office Action – page 6). The applicants respectfully disagree.

This portion of Springer, as discussed above, merely discloses how to process incoming address signals N with respect to an odd and even memory module. This portion of Springer, however, does not disclose alternately transferring data as recited in claim 18. If the Examiner persists in this argument, the applicants respectfully request that the Examiner explain how this portion of Springer can be construed to disclose alternately transferring data received from a first multiplexer to first and second external memory buses and alternately transferring data received from a second multiplexer to the first and second external memory buses, as required by claim 18.

In any event, Springer does not disclose or suggest the features recited in claim 18. For at least these additional reasons, withdrawal of the rejection and allowance of claim 18 are respectfully requested.

Claims 2-6 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell in view of Springer and further in view of Gayton et al. (U.S. Patent No. 5,680,401; hereinafter Gayton). The rejection is respectfully traversed.

Claims 2-6 and 12 depend on claims 1 and 10, respectively, and are believed to be allowable for at least the reasons their respective independent claims are allowable. Gayton does not make up for the deficiencies in the combination of Hassell and Springer discussed

above with respect to claims 1 and 10. Accordingly, withdrawal of the rejection and allowance of claims 2-6 and 12 are respectfully requested.

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell in view of Springer in view of Gayton and further in view of Runaldue et al. (U.S. Patent No. 6,052,751; hereinafter Runaldue). The rejection is respectfully traversed.

Claim 7 depends on claim 1 and is believed to be allowable for at least the reasons claim 1 is allowable. Runaldue does not make up for the deficiencies in the combination of Hassell and Springer discussed above with respect to claim 1. Accordingly, withdrawal of the rejection and allowance of claim 7 are respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, the applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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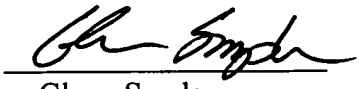
By: 
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